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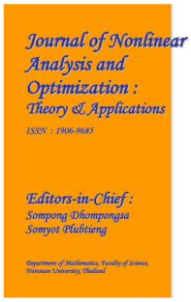

EFFICIENT SEGMENTED ΣΔ-DAC ARCHITECTURE FOR BIST PROGRAMMABLE DC VOLTAGE GENERATORS

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Abstract
This project introduces a segmented architecture for Sigma-delta (ΣΔ) digital-to-analog converters (DACs), tailored for integration into built-in self-test (BIST) schemes for programmable DC voltage generators. While ΣΔ-DACs offer high linearity, they are challenged by significant digital memory requirements and the need for large reconstruction filters, which consume substantial silicon area. The proposed segmented DAC architecture addresses these limitations by employing two sub-DACs, both leveraging ΣΔ technology. This approach offers two primary benefits: it reduces the footprint size of the reconstruction filter and achieves substantial memory savings, simplifying BIST implementation. Two experimental prototypes validate the efficacy of the segmented ΣΔ-DAC approach. The first prototype, an integrated circuit (IC) design, achieves 12 bits of resolution with just 1020 memory elements, compared to 4095 elements required by an unsegmented ΣΔ-DAC for the same resolution. The second prototype implements the segmented architecture using discrete components, achieving an impressive 16 bits of resolution with only 1020 memory elements, in contrast to the 65,535 bits needed by the unsegmented counterpart. This significant reduction in memory elements underscores the efficiency of the segmented approach. In conclusion, this project demonstrates the effectiveness of the segmented ΣΔ-DAC architecture, showcasing substantial memory and silicon area savings compared to traditional unsegmented designs. These advantages position it as a compelling solution for programmable DC voltage generators in BIST schemes, offering enhanced efficiency and performance.

Keywords:
Segmented ΣΔ-DAC, Built-In Self-Test (BIST), Digital-to-Analog Converter (DAC), Sigma-delta (ΣΔ) technology, Programmable DC Voltage Generators, High Linearity, Memory Savings, Silicon Area Reduction.

1 Introduction

The use of programmable DC voltage generators in built-in self-test (BIST) schemes for mixed-signal integrated circuits is crucial for efficient testing and fault detection. These generators typically rely on high-resolution digital-to-analog converters (DACs) to produce slow-changing, short-term analog DC levels. Unlike traditional DACs that prioritize dynamic measures like signal-to-noise ratio (SNR) and total harmonic distortion (THD), DACs used in programmable DC generators for BIST focus on integral nonlinearity (INL) and differential nonlinearity (DNL) metrics. The emphasis on INL and DNL is due to the necessity of correcting process variations in semiconductor fabrication. These variations can significantly impact the performance of DACs and ultimately affect the accuracy of voltage levels generated during testing. Calibration for supply voltage and temperature fluctuations would incur excessive area overhead, making it impractical for BIST applications. To address voltage supply variations, a practical approach involves powering up the BIST using stable power supply levels provided by simple test equipment. Temperature variations, on the other hand, are generally insignificant for DACs used in BIST since they operate only during the testing phase and not for extended periods. DACs intended for testing purposes are calibrated to specifically account for process variations, ensuring accurate voltage generation during BIST. Techniques described in literature ([7]-[9]) focus on optimizing DAC performance for BIST applications, considering factors such as area efficiency, process variation compensation, and stability under varying operating conditions. Overall, the integration of programmable DC voltage generators with optimized DACs into BIST schemes enables manufacturers to conduct thorough testing of mixed-signal ICs while minimizing costs and maintaining the precision required for modern semiconductor devices. Dynamic Element Matching (DEM) techniques are essential for managing matching errors in digital-to-analog converters (DACs) by dynamically reorganizing interconnections among mismatched elements. This ensures that the average values of the elements are nearly equal, enhancing the overall performance of the DAC. However, implementing high-resolution DEM DACs introduces complexity, particularly in handling binary data inputs and transforming them into thermometer codes, as noted in literature ([4], [10]). As the resolution of DACs increases, the complexity of the encoding process grows exponentially, posing a significant challenge in hardware design. Addressing this challenge, Jiang et al. proposed an approach that involved utilizing two 8-bit deterministic DEM DACs to test 12-bit Analog-to-Digital Converters (ADCs) without the need for special signal processing ([11]). However, this technique is not extensively adopted for testing higher-resolution ADCs due to the requirement for high-resolution DEM DACs. The method proposed by Jiang et al. in [11] is specifically tailored for histogram-based linearity testing of ADCs. While it provides a solution for testing ADCs without necessitating complex signal processing, it may not be suitable for testing ADCs with resolutions beyond 12 bits due to limitations in the resolution of DEM DACs. Overall, DEM techniques offer a means to manage matching errors in DACs, but their implementation becomes increasingly complex as DAC resolution rises. While approaches like the one proposed by Jiang et al. provide solutions for specific testing scenarios, further research is needed to address challenges associated with testing higher-resolution ADCs using DEM techniques. An alternative to traditional DAC architectures is the pulse-width modulated (PWM) DAC, which encodes its output in the duty cycle of a PWM digital bitstream. This bitstream is then averaged by a low-pass filter (LPF) to generate the desired DC output. PWM DACs offer high linearity but suffer from a significant drawback—the substantial size of the LPF. For instance, in [20], it was found that the LPF occupies approximately 60% of the silicon area of an 8-bit PWM DAC, making PWM DACs less favorable for built-in self-test (BIST) applications. To address this issue, studies [20] and [21] demonstrated the use of pulse density modulated digital bitstreams, known as PDM DACs, which allow for the utilization of LPFs with higher cut-off frequencies. This reduction in LPF size makes PDM DACs more attractive compared to PWM DACs. PDM DACs are sometimes referred to as ΣΔ-DACs since the PDM bitstream is generated using sigma-delta modulators. Both segmented and unsegmented ΣΔ-DACs have found extensive usage in testing applications ([6], [22]-[25]). However, unsegmented ΣΔ-DACs face the challenge of requiring filters with a substantial silicon area footprint. Additionally, the memory-based ΣΔ-DAC approach ([26]) encounters issues due to the necessity for numerous memory elements to store the DAC input codes. In this context, a novel segmented architecture for a 16-bit digital-to-analog converter (DAC) is introduced. In this design, segmentation occurs before the sigma-delta (ΣΔ) modulation operation,

followed by two independent all-digital ΣΔ modulation operations and their corresponding digital-to-analog conversion operations. The innovative approach of this design reduces the number of bits per period compared to conventional unsegmented ΣΔ-DACs. This shift effectively moves the fundamental frequency away from the signal of interest, enabling a reduction in the size of the required filter. Moreover, the decrease in the number of bits per period leads to significant memory savings when implementing the memory-based approach. The article aims to experimentally demonstrate the advantages of using the proposed segmented ΣΔ-DAC over traditional unsegmented counterparts, particularly in terms of silicon area footprint, filter size, and memory requirements. This advancement could potentially enhance the efficiency and effectiveness of DACs in BIST applications and other testing scenarios.

2 Literature Survey

Shim et.al [1] The proposed segmented butterfly shufflers technique offers a solution to the challenge of LO leakage in RF transmitters. This technique involves dividing the digital signal into segments and processing them using the butterfly shuffler algorithm, which efficiently mitigates LO leakage. By segmenting the digital signal, the proposed architecture optimizes the performance of the RF transmitter, leading to reduced LO leakage and enhanced signal quality. LO leakage, which occurs due to the leakage of the local oscillator (LO) signal into the output spectrum, is a common issue in RF transmitters that can degrade signal quality and interfere with neighbouring frequency bands. The butterfly shuffler algorithm is known for its effectiveness in suppressing LO leakage by carefully arranging the phase relationships between the LO and the input signal. Segmenting the digital signal before processing it with the butterfly shuffler algorithm allows for better control and optimization of the signal processing. By dividing the signal into segments, each segment can be individually processed to ensure that LO leakage is effectively suppressed across the entire spectrum of the output signal.

Sun et.al [2] The paper presents a novel approach aimed at designing high-order mismatch-shaped segmented multibit delta sigma digital-to-analog converters (DACs) with arbitrary unit weights. The primary goal of this approach is to enhance the linearity and performance of the DAC while minimizing the impact of mismatch errors that can adversely affect the accuracy of the DAC's output. To achieve this objective, the proposed architecture combines segmentation and multibit delta sigma modulation techniques. Segmentation involves dividing the DAC into smaller sections, allowing for more precise control over the conversion process. Multibit delta sigma modulation techniques are utilized to further refine the conversion process, improving the resolution and accuracy of the DAC output. By employing segmented multibit DACs, the design optimizes both the resolution and accuracy of the DAC output. Segmenting the DAC enables finer control over the conversion process, leading to improved linearity and reduced errors in the output signal.

Liu et.al [3] implements paper likely provides a comprehensive examination of the design methodology employed to implement the proposed gradient error suppression techniques in an 8-bit string digital-to-analog converter (DAC). It is probable that the paper offers a detailed explanation of the theoretical framework underpinning the proposed techniques, including circuit designs, signal processing algorithms, and calibration methodologies aimed at mitigating gradient errors. Furthermore, the paper is expected to present experimental results obtained from simulations and practical implementations to validate the effectiveness of the proposed techniques. These results may include measurements of linearity, distortion, and other relevant performance metrics, showcasing the improvements achieved by the gradient error suppression techniques. Additionally, the paper likely provides comparisons with existing methods or conventional DAC designs to highlight the advantages of the proposed approach in terms of enhanced linearity and overall performance. Through this thorough analysis, the paper aims to establish the efficacy of the proposed gradient error suppression techniques in enhancing linearity and advancing the state-of-the-art in digital-to-analog conversion technology.

3 Methodology

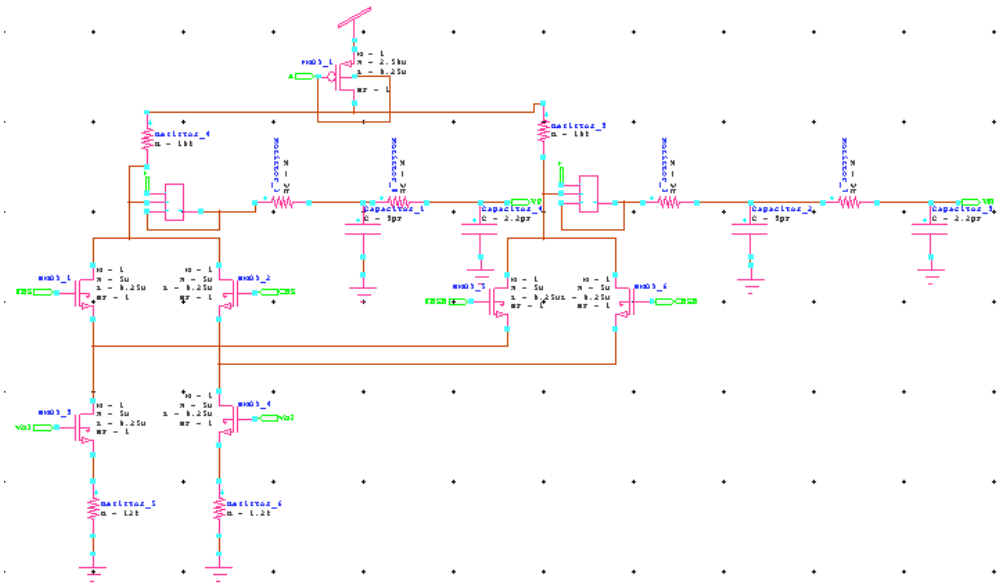

Fig 1 Schematic of sigma delta DAC using power gating

LM317s are adjustable linear voltage regulators that are commonly used to provide a stable output voltage from an unregulated input voltage. Here's a breakdown of the circuit's components and their functionalities:

- **Input Capacitor (C1):** This capacitor helps to smooth out any fluctuations or ripples in the input voltage source.
- **Resistor (R1):** This resistor along with R2 and the variable resistor (VR1) set the output voltage of the LM317 voltage regulator. By adjusting VR1, you can control the output voltage.
- **Variable Resistor (VR1):** This component allows you to manually adjust the output voltage of the circuit.
- **LM317 Voltage Regulator:** This is the core voltage regulator component. It takes the unregulated input voltage and provides a stable output voltage based on the settings of R1, R2, and VR1.
- **Output Capacitor (C2):** This capacitor helps to minimize any noise or voltage spikes at the output of the voltage regulator
- **LED (Light Emitting Diode):** The LED is likely used as a visual indicator that the circuit is functioning properly. It will illuminate when the output voltage is within the desired range.
- **Resistor (R3):** This resistor limits the current flowing through the LED, protecting it from damage. Overall, this circuit is a basic adjustable voltage regulator circuit that can be used to provide a stable output voltage from an unregulated input voltage source. The variable resistor allows you to adjust the output voltage to meet your specific needs.

Results

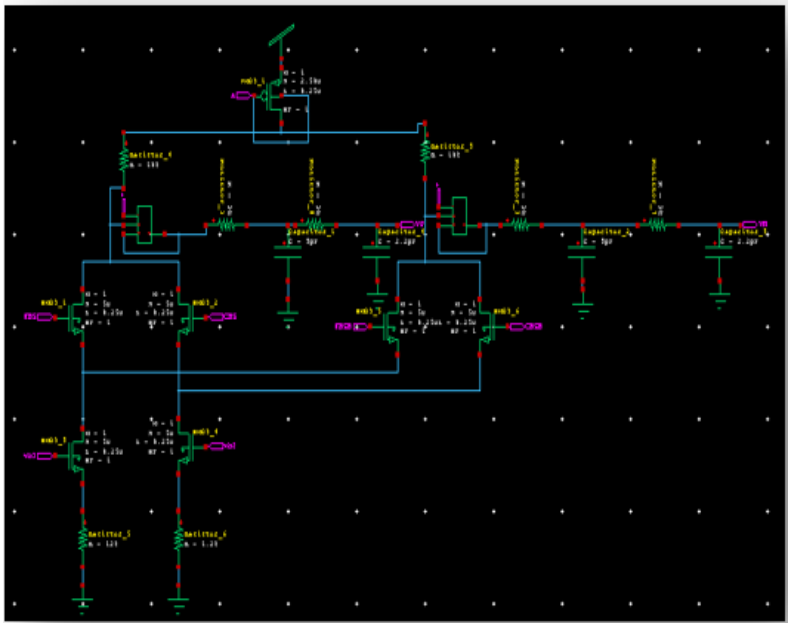

Fig 2 SCHEMATIC OF PROPOSED SIGMA DELTA DAC

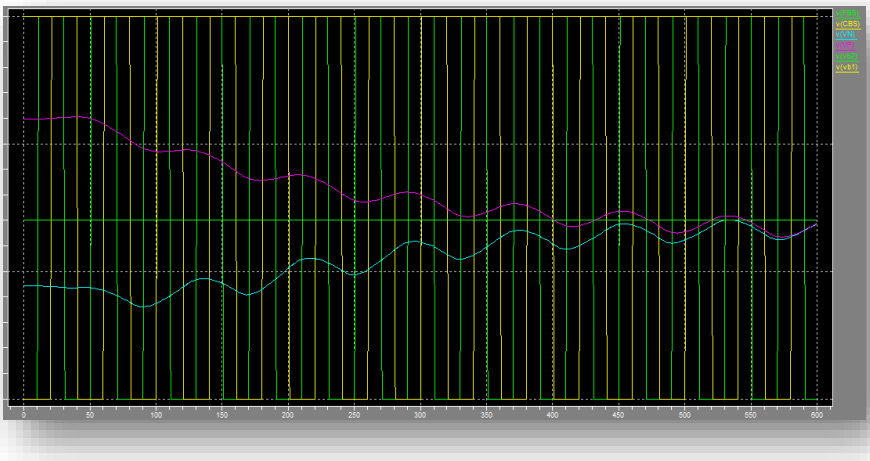

FIG 3 WAVEFORM OF PROPOSED METHOD

Conclusion

In conclusion, this project introduces a segmented architecture for Sigma-delta (ΣΔ) digital-to-analog converters (DACs) tailored for integration into built-in self-test (BIST) schemes for programmable DC voltage generators. Traditional ΣΔ-DACs face challenges such as significant digital memory requirements and the need for large reconstruction filters, consuming substantial silicon area. The proposed segmented DAC architecture overcomes these limitations by employing two sub-DACs, leveraging ΣΔ technology. This approach yields two primary benefits: reducing the footprint size of the reconstruction filter and achieving substantial memory savings, simplifying BIST implementation. Experimental prototypes validate the efficacy of the segmented ΣΔ-DAC approach, demonstrating impressive resolution with minimal memory elements compared to unsegmented designs. This significant reduction in memory elements highlights the efficiency of the segmented approach, positioning it as a compelling solution for programmable DC voltage generators in BIST schemes, offering enhanced efficiency and performance.

Future Scope

The proposed segmented ΣΔ-DAC architecture offers a novel approach for built-in self-test (BIST) programmable DC voltage generators, addressing challenges such as high memory requirements and large silicon area consumption associated with traditional designs. By employing two sub-DACs leveraging ΣΔ technology, this architecture achieves significant memory savings and reduces the

footprint of reconstruction filters while maintaining high resolution. Experimental prototypes demonstrate impressive performance, positioning the segmented approach as an efficient solution for enhancing the efficiency and functionality of BIST schemes in programmable DC voltage generators**.**

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